

ABSTRACT OF THE DISCLOSURE

An image processing circuit is provided in which
a clock signal is divided according to bits of data
input thereto and supply or interruption of the divided
clock signals is controlled according to the value of
the input data. Therefore, it becomes possible to
interrupt the clock signal which is to be supplied for
a bit among the bits of the input data which is not
used for a long period of time and reduce the power
consumption of the circuit.

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